What is Claimed is:

1. A magnetic random access memory (MRAM) device structure having a main cell region and a reference cell region adjacent to the main cell region, the MRAM device structure comprising:

a plurality of main magnetic resistors disposed in the main cell region along rows and columns, each of the main magnetic resistors having a first width and a first length when viewed from a plan view; and

a plurality of reference magnetic resistors disposed in the reference cell region along a column, each of the reference magnetic resistors having a second width and a second length, a length direction of the main magnetic resistors intersecting a length direction of the main magnetic resistors at a predetermined nonzero angle.

2. The MRAM device structure of Claim 1, wherein the first and second lengths are greater than the first and second widths respectively, and each of the main magnetic resistors and the reference magnetic resistors has a rectangular shape or an oval shape when viewed from a plan view.

3. The MRAM device structure of Claim 1, wherein each of the main magnetic resistors comprises a main bottom electrode, a main magnetic tunnel junction (MTJ) structure and a main top electrode, which are sequentially stacked, and each of the reference magnetic resistors comprises a reference bottom electrode, a reference MTJ structure and a reference top electrode, which are sequentially stacked.

4. The MRAM device structure of Claim 3, wherein the main MTJ structure comprises a main pinning layer, a main pinned layer, a main tunneling layer and a main free layer, which are sequentially stacked, and the reference MTJ structure comprises a reference pinning layer, a reference pinned layer, a reference tunneling layer and a reference free layer, which are sequentially stacked.

5. The MRAM device structure of Claim 1, wherein the predetermined nonzero angle is 90°.

6. The MRAM device structure of Claim 1 further comprising a reference bit line disposed in the reference cell region, wherein the reference bit line is extends parallel to a column, and the reference bit line is electrically connected to top surfaces of the reference magnetic resistors which are one dimensionally arrayed along a column under the reference bit line.

7. The MRAM device structure of Claim 1 further comprising a plurality of parallel main bit lines disposed in the main cell region, wherein the main bit lines are parallel to the columns, and each of the main bit lines is electrically connected to top surfaces of the main magnetic resistors which are one dimensionally arrayed along the column under the respective main bit lines.

8. The MRAM device structure of Claim 1 further comprising a plurality of parallel digit lines disposed under the main magnetic resistors and the reference magnetic resistors, wherein the digit lines extend parallel to the rows and are insulated from the main magnetic resistors and the reference magnetic resistors.

9. The MRAM device structure of Claim 1, further comprising:

a plurality of main access transistors in the main cell region and electrically connected to bottom surfaces of the main magnetic resistors, respectively; and

a plurality of reference access transistors in the reference cell region and electrically connected to bottom surfaces of the reference magnetic resistors, respectively.

10. The MRAM device structure of Claim 9, wherein the main access transistors and the reference access transistor, which are arrayed in the respective rows, share a single word line.

11. A magnetic random access memory (MRAM) device structure including a main cell region and a reference cell region, which are defined in a semiconductor substrate, the main cell region having a plurality of main cells disposed along rows and columns, the reference cell region having a plurality of reference cells disposed along a column, the MRAM device structure comprising:

a plurality of digit lines extending parallel to the columns on the semiconductor substrate;

a plurality of main bit lines disposed in the main cell region, the main bit lines crossing over the digit lines;

a reference bit line disposed in the reference cell region, the reference bit line crossing over the digit lines;

a plurality of main magnetic resistors interposed between the main bit lines and the digit lines, each of the main magnetic resistors having a width and a length greater than the width when viewed from a plan view, the main magnetic resistors extending parallel to a single direction; and

a plurality of reference magnetic resistors interposed between the reference bit line and the digit lines, the reference magnetic resistors having same configuration and structure as the main magnetic resistors and extending perpendicular to the single direction.

12. The MRAM device structure of Claim 11, wherein each of the main magnetic resistors and the reference magnetic resistors has a rectangular shape or an oval shape when viewed from a plan view.

13. The MRAM device structure of Claim 11, wherein each of the main magnetic resistors comprises a main bottom electrode, a main magnetic tunnel junction (MTJ) structure and a main top electrode which are sequentially stacked, and each of the reference magnetic resistors comprises a reference bottom electrode, a reference MTJ structure and a reference top electrode which are sequentially stacked, the reference bit line being electrically connected to the reference top electrodes.

14. The MRAM device structure of Claim 13, wherein each of the main MTJ structures comprises a main pinning layer, a main pinned layer, a main tunneling layer and a main free layer which are sequentially stacked, and each of the reference MTJ structures comprises a reference pinning layer, a reference pinned layer, a reference tunneling layer and a reference free layer which are sequentially stacked.

15. The MRAM device structure of Claim 11, wherein the digit lines are insulated from the main magnetic resistors and the reference magnetic resistors.

16. The MRAM device structure of Claim 13, wherein each of the main bit lines are electrically connected to the main top electrodes thereunder, and the reference bit line is electrically connected to the reference top electrodes thereunder.

17. The MRAM device structure of Claim 13, further comprising:

a plurality of main access transistors having drain regions which are respectively connected to the main bottom electrodes; and

a plurality of reference access transistors having drain regions which are respectively connected to the reference bottom electrodes.

18. A magnetic random access memory (MRAM) device comprising:

a reference bit line;

a plurality of reference cells connected in parallel to the reference bit line, each of the reference cells comprising a single reference access transistor and a single reference magnetic resistor which are serially connected, each of the reference magnetic resistors having a first terminal electrically connected to the reference bit line and a second terminal electrically connected to a respective reference access transistor; and

a sense amplifier electrically connected to the reference bit line.

19. The MRAM device of Claim 18 further comprising a plurality of word lines electrically connected to gate electrodes of the reference access transistors, respectively.

20. The MRAM device of Claim 19 further comprising a plurality of main bit lines that are also electrically connected to the sense amplifier.

21. The MRAM device of Claim 20 further comprising a plurality of main cells connected in parallel to the respective main bit lines, wherein each of the main cells comprises a single main access transistor and a single main magnetic resistor which are serially connected, each of the main magnetic resistors having a first terminal electrically connected to one of the main bit lines and a second terminal electrically connected to a respective main access transistor.

22. The MRAM device of Claim 21, wherein each of the word lines is electrically connected to gate electrodes of the main access transistors that extend adjacent thereto.

23. The MRAM device of Claim 21, wherein source regions of the main access transistors and the reference access transistors are electrically connected to a common source line.

24. The MRAM device of Claim 21 further comprising a plurality of digit lines in the main cell array portion.

25. The MRAM device of Claim 21, wherein each of the reference magnetic resistors has a resistance that corresponds to a mid-value between a maximum resistance and a minimum resistance of the main magnetic resistors.

26. A Magnetic Random Access Memory (MRAM) comprising:
an MRAM substrate including a face;
a plurality of elongated main magnetic resistors that extend along the face; and
a plurality of elongated reference magnetic resistors that extend along the face nonparallel to the plurality of elongated main magnetic resistors.

27. The MRAM of Claim 26 wherein the plurality of elongated reference magnetic resistors extend along the face orthogonal to the plurality of elongated main magnetic resistors.

28. The MRAM of Claim 26 wherein the plurality of elongated reference magnetic resistors and the plurality of elongated main magnetic resistors are rectangular or oval shaped.

29. The MRAM of Claim 26 wherein the plurality of elongated main magnetic resistors are configured to have a maximum resistance or a minimum resistance and wherein the plurality of elongated reference magnetic resistors are

configured to have resistance between the maximum resistance and the minimum resistance.

30. The MRAM of Claim 26 wherein the plurality of elongated main magnetic resistors are configured to have a maximum resistance or a minimum resistance and the wherein the plurality of elongated reference magnetic resistors are configured to have resistance midway between the maximum resistance and the minimum resistance.

31. The MRAM of Claim 26 wherein the plurality of elongated reference magnetic resistors and the plurality of elongated main magnetic resistors each include a pinned layer having magnetic spins that are oriented parallel to one another along the face.

32. The MRAM of Claim 26 further comprising:

a plurality of main access transistors, a respective one of which is connected to a respective one of the plurality of elongated main magnetic resistors to define a plurality of main cells, each of which comprises a single main access transistor and a single main magnetic resistor; and

a plurality of reference access transistors, a respective one of which is connected to a respective one of the plurality of elongated reference magnetic resistors to define a plurality of reference cells, each of which comprises a single reference access transistor and a single reference magnetic resistor.

33. The MRAM of Claim 32 further comprising:

a common line;

a main bit line; and

a reference bit line;

wherein at least one of the main cells is connected between the common line and the main bit line and at least one of the reference cells is connected between the common line and the reference bit line.

34. The MRAM of Claim 33 further comprising:

a word line;

wherein the at least one of the main cells that is connected between the common line and the main bit line and the at least one of the reference cells that is connected between the common line and the reference bit line are also connected to the word line.

35. The MRAM of Claim 34 wherein the common line and the word line extend along the face parallel to one another and wherein the main bit line and the reference bit line extend along the face parallel to one another and nonparallel to the common line and the word line.

36. The MRAM according to Claim 33 further comprising:

a sense amplifier that is connected between the main bit line and the reference bit line.

37. A Magnetic Random Access Memory (MRAM) comprising:

an MRAM substrate;

a plurality of main magnetic resistors and a plurality of main access transistors on the substrate, the main magnetic resistors being configured to have a maximum resistance or a minimum resistance, a respective one of the main magnetic resistors being connected to a respective one of the plurality of main access transistors to define a plurality of main cells, each of which comprises a single main access transistor and a single main magnetic resistor; and

a plurality of reference magnetic resistors and a plurality of reference access transistors on the substrate, the reference magnetic resistors being configured to have resistance between the maximum resistance and the minimum resistance, a respective one of the reference magnetic resistors being connected to a respective one of the plurality of reference access transistors to define a plurality of reference cells, each of which comprises a single reference access transistor and a single reference magnetic resistor.

38. The MRAM of Claim 37 wherein the MRAM substrate includes a face, wherein the plurality of main magnetic resistors comprise a plurality of elongated main magnetic resistors, wherein the plurality of reference magnetic resistors comprise a plurality of elongated reference magnetic resistors, and wherein the

plurality of elongated main magnetic resistors extend along the face and the plurality of elongated reference magnetic resistors extend along the face nonparallel to the plurality of elongated main magnetic resistors.

39. The MRAM of Claim 38 wherein the plurality of elongated reference magnetic resistors extend along the face orthogonal to the plurality of elongated main magnetic resistors.

40. The MRAM of Claim 38 wherein the plurality of elongated reference magnetic resistors and the plurality of elongated main magnetic resistors are rectangular or oval shaped.

41. The MRAM of Claim 37 wherein the plurality of reference magnetic resistors are configured to have resistance midway between the maximum resistance and the minimum resistance.

42. The MRAM of Claim 37 wherein the plurality of reference magnetic resistors and the plurality of main magnetic resistors each include a pinned layer having magnetic spins that are oriented parallel to one another.

43. The MRAM of Claim 37 further comprising:

a common line;

a main bit line; and

a reference bit line;

wherein at least one of the main cells is connected between the common line and the main bit line and at least one of the reference cells is connected between the common line and the reference bit line.

44. The MRAM of Claim 43 further comprising:

a word line;

wherein the at least one of the main cells that is connected between the common line and the main bit line and the at least one of the reference cells that is connected between the common line and the reference bit line are also connected to the word line.

45. The MRAM of Claim 44 wherein the common line and the word line extend parallel to one another and wherein the main bit line and the reference bit line extend parallel to one another and nonparallel to the common line and the word line.

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46. The MRAM according to Claim 43 further comprising:

a sense amplifier that is connected between the main bit line and the reference bit line.